

Wide Bandgap Semiconductor Technology Initiative: High Power Electronics (HPE)

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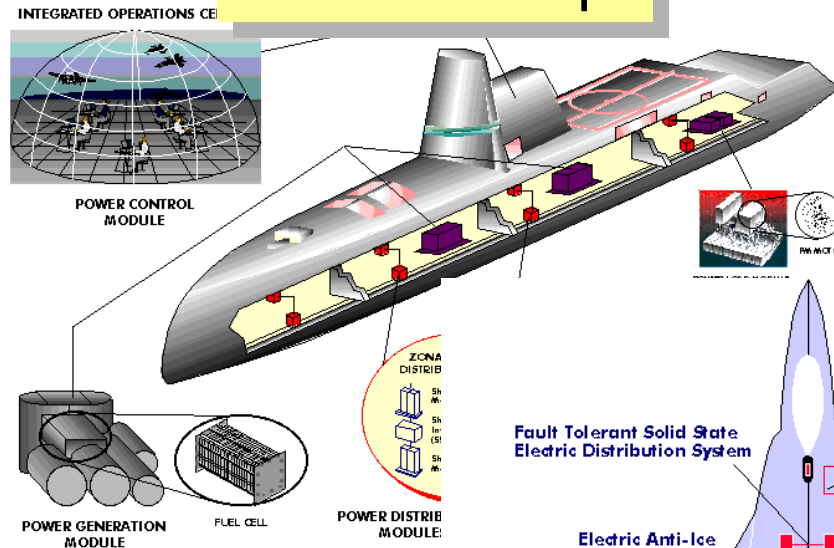
**Wide Bandgap Kickoff
Meeting**

21 - 22 May 2002

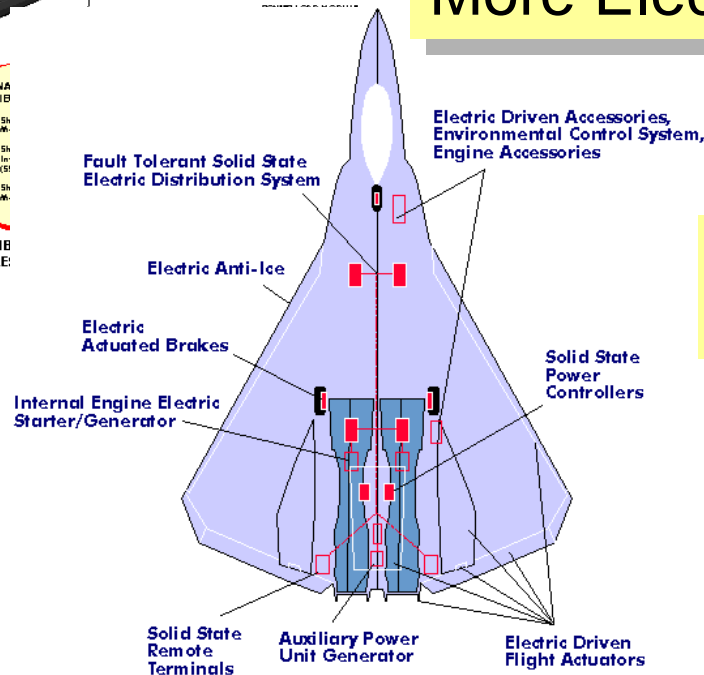


WBG High Power Electronics: enabler for future “electric force”

Electric Ship



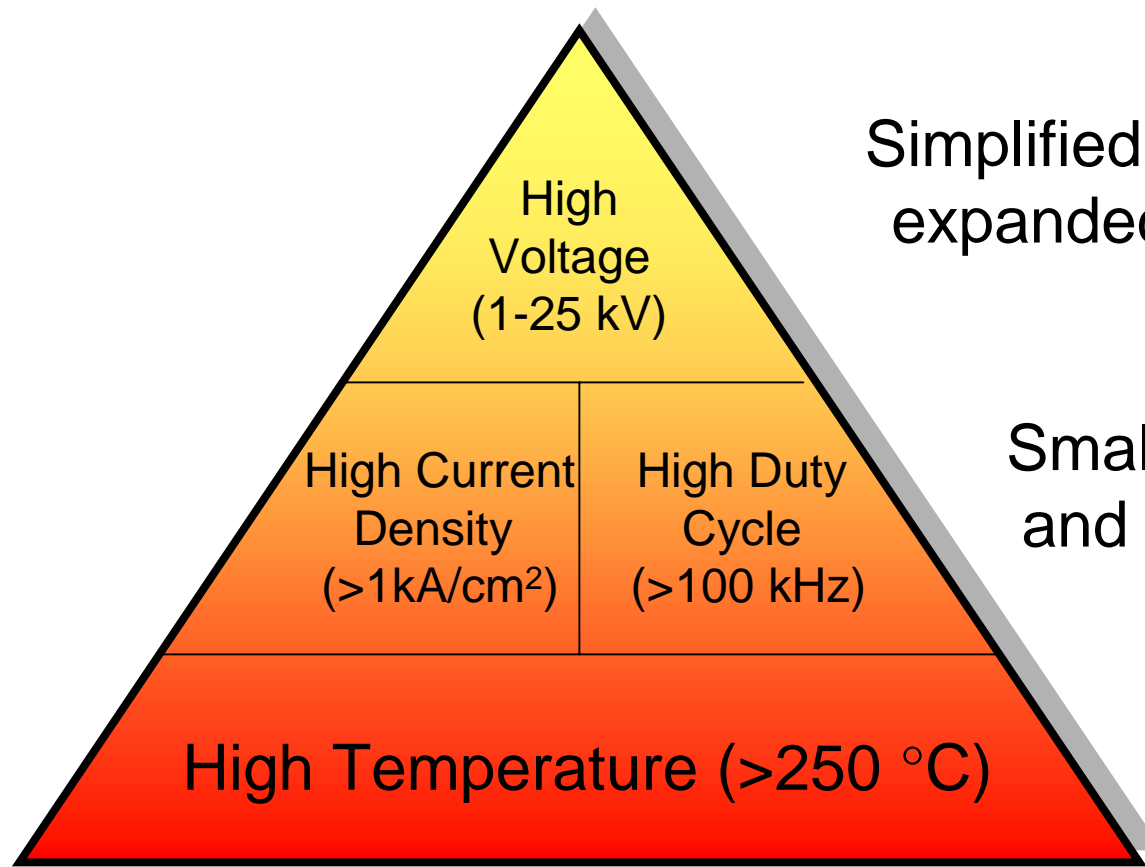
More Electric Aircraft



All Electric Combat Vehicle (AECV)



Wide Bandgap High Power Electronics (HPE)



Simplified circuits and expanded capability

Smaller, lower loss, active and passive components

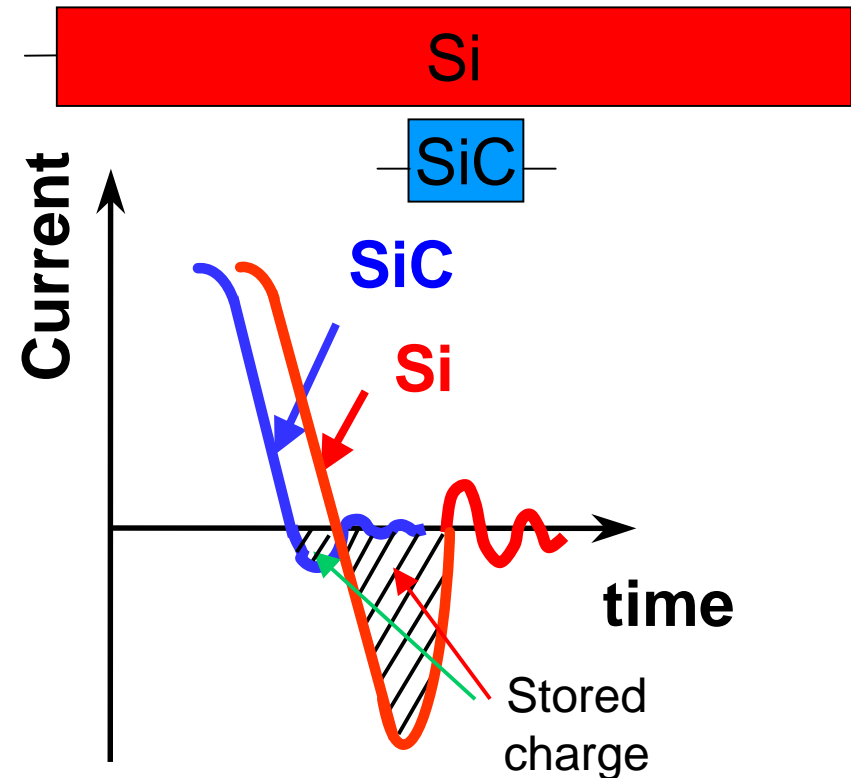
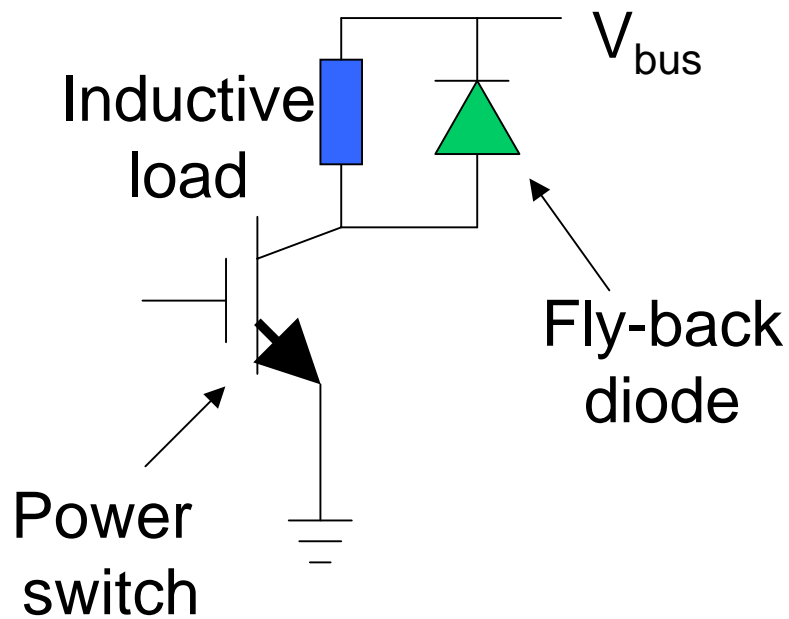
Smaller cooling systems

Silicon Carbide



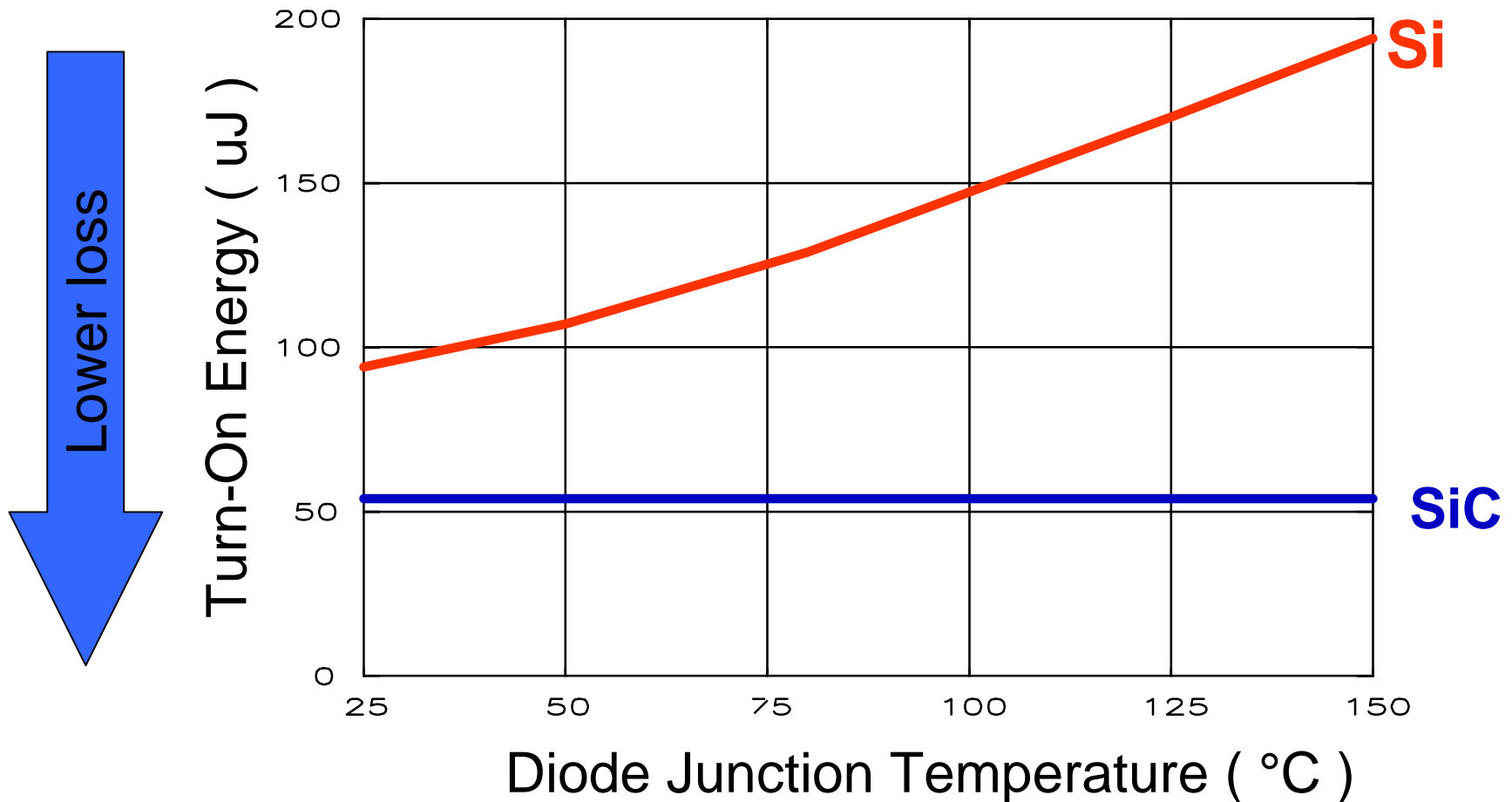
SiC Reduces Switching Losses

Motor Drive



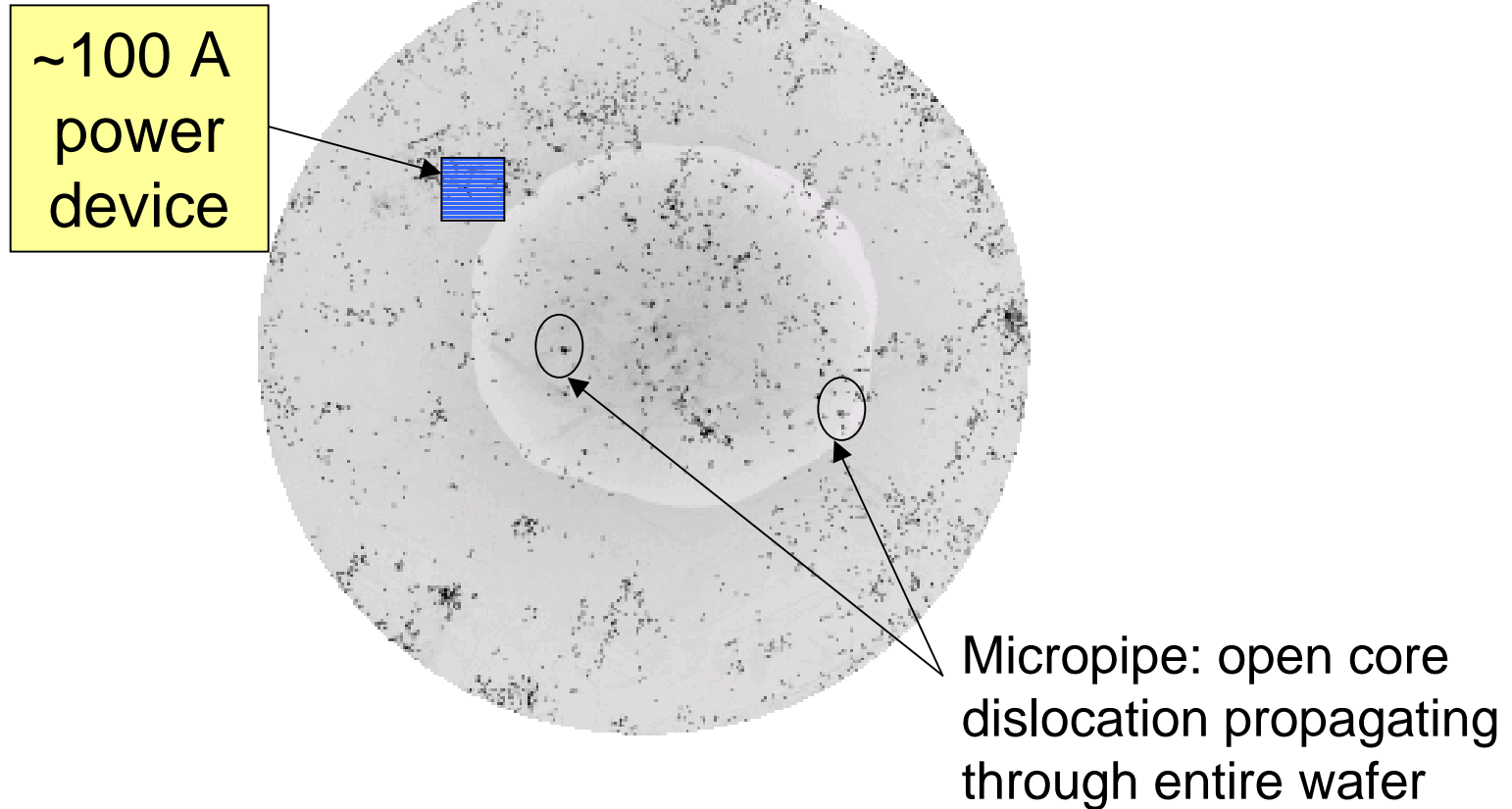
Diode switching characteristics

High Temperature Operation



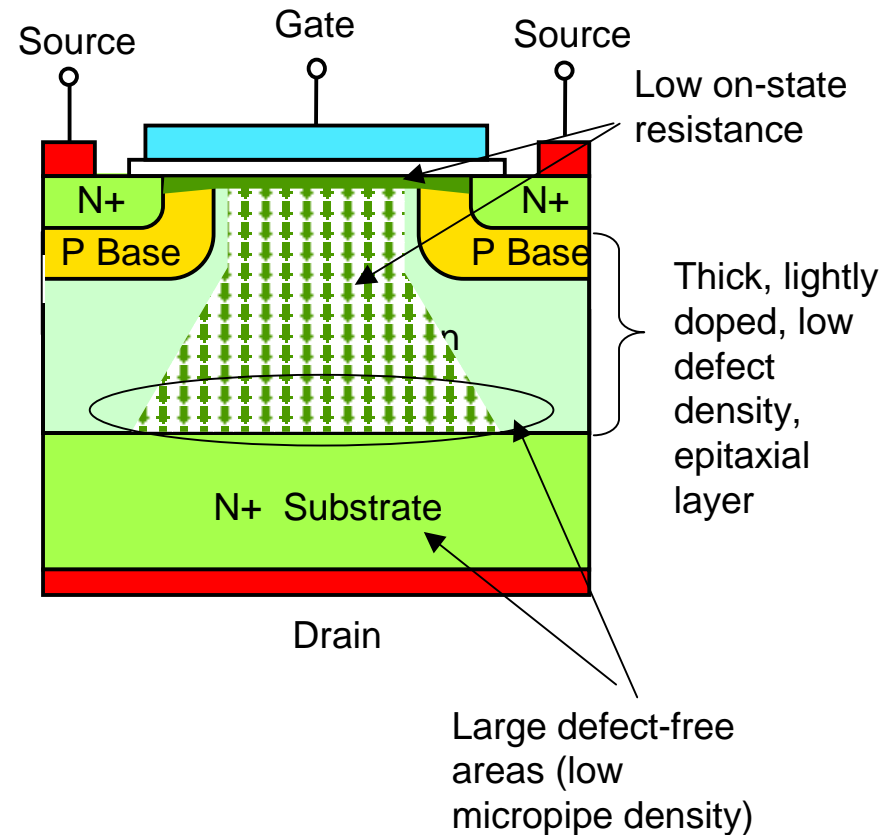
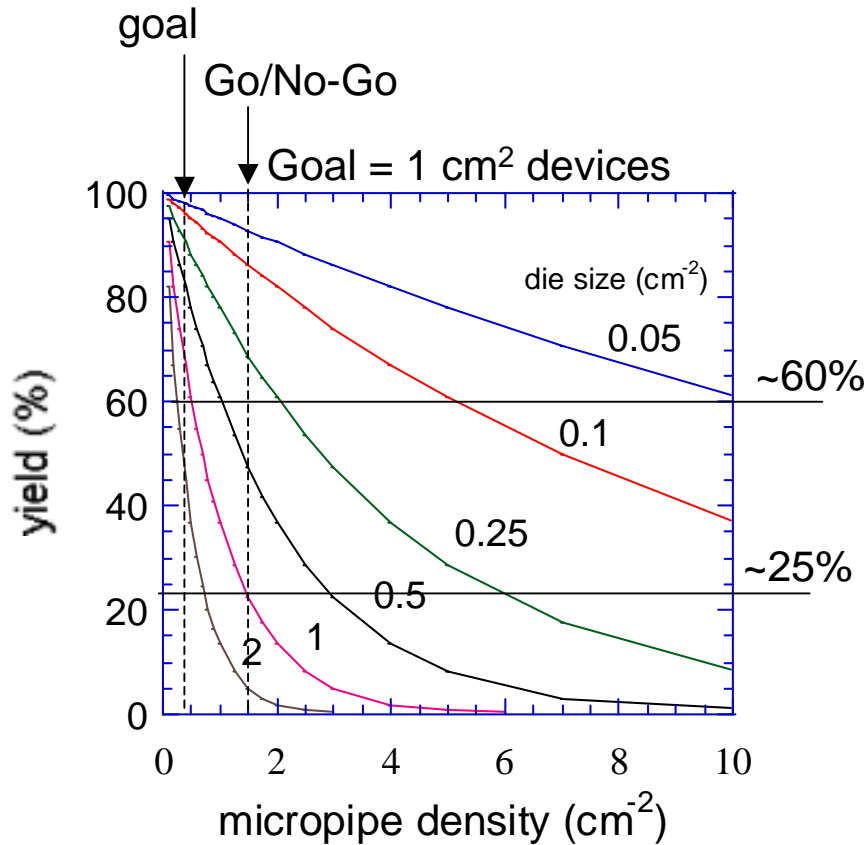
High temperature operation reduces cooling requirements and system cost

Critical Challenge: Material Quality for Large Area Devices



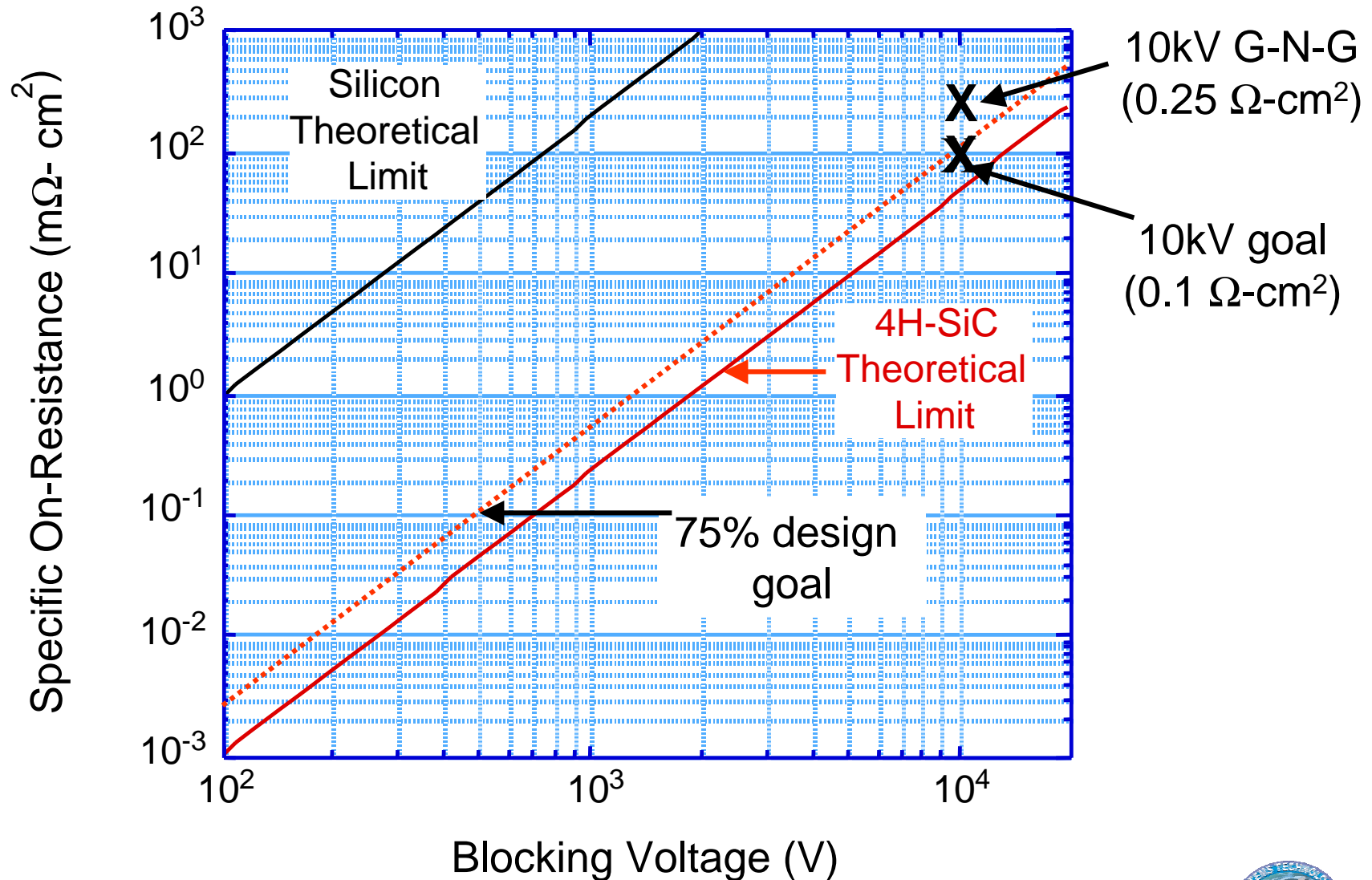
Defect etch of 75mm wafer (n-type)

Phase I Technical Challenges

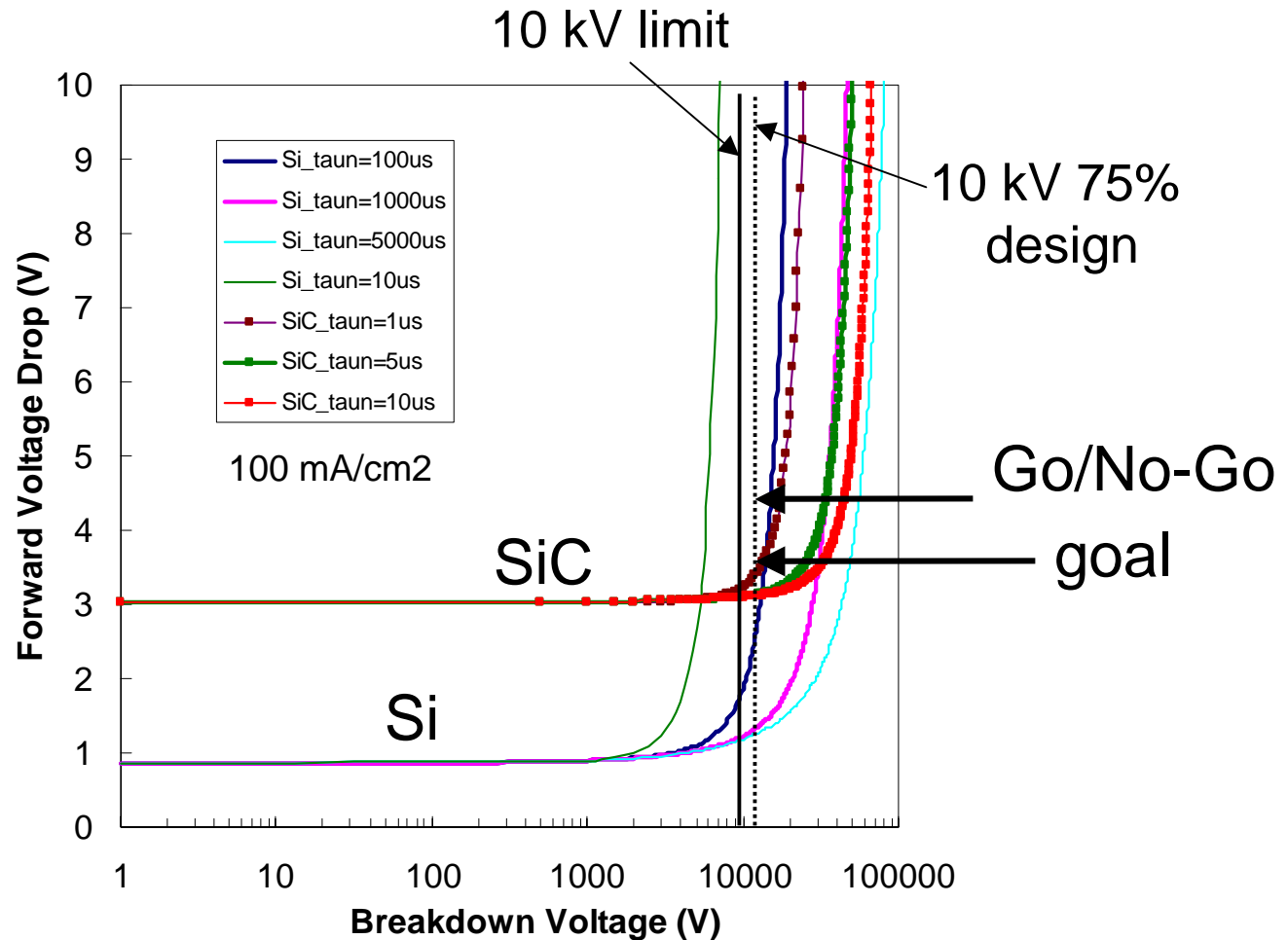


SiC Power Transistor

On-state characteristics: FET



SiC PIN diode on state voltage



Semiconductor resistance only,
Parasitic contact resistance not included

HPE Milestones

task	12-18m	Goal
1. SiC substrate	(a) < 1 micropipes/cm² for 3 inch ; (b) < 10 micropipe/cm² for 4 inch	(a) < 0.2 micropipes/cm² for 3 inch ; (b) < 1.0 micropipes/cm² for 4 inch
2. SiC substrate	(a) < 500 dislocations/cm² for 3 inch ; (b) < 1000 dislocations/cm² for 4 inch	(a) < 50 dislocations/cm² for 3 inch ; (b) < 100 dislocations/cm² for 4 inch
3. Thick epi	100 um epi with < 5% thickness and doping variation at 5x10¹⁴cm⁻³ with < 1.5 total electrically active defects/cm² on 3 inch;	150 um epi with < 5% thickness and doping variation at 1x10¹⁴cm⁻³ with < 0.5 total electrically active defects/cm² on 3 inch ;

Red = primary milestones

HPE Milestones-2

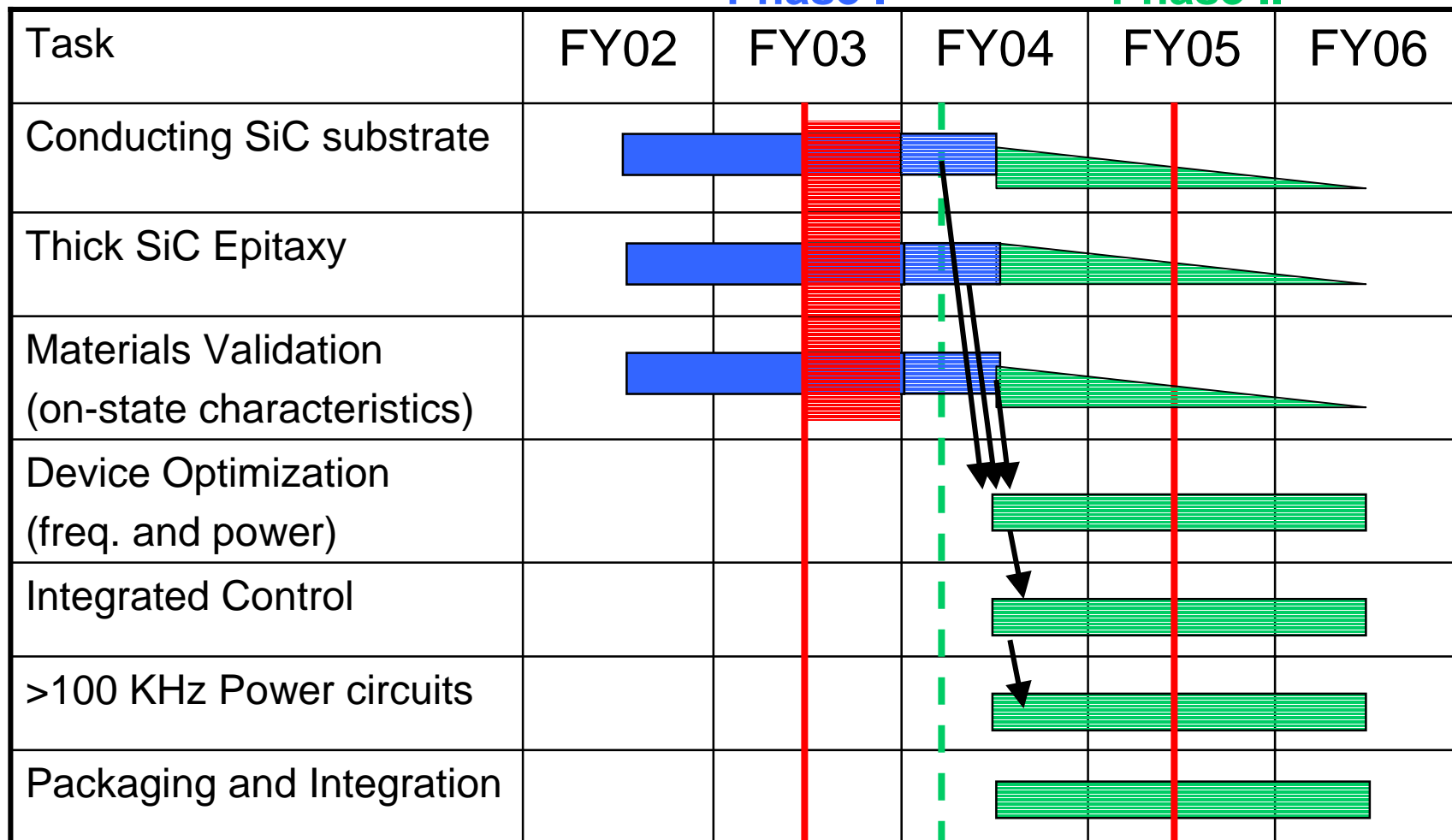
task	12-18m	Goal
4. PIN on-state	10 kV, PIN with $V_f < 4.5$ V at 100 A/cm² (≥ 50 A total current) with <100 mV drift over 100 hours	10 kV, PIN with $V_f \leq 3.5$ V at 100 A/cm ² (≥ 50 A total current) with <100 mV drift over 100 hours
5. FET on-state	0.25 ohm-cm² with 10 kV blocking	0.10 ohms-cm ² with 10 kV blocking
6. mobility	100 cm ² /V-s in implanted p-well	200 cm ² /V-s in implanted p-well

Red = primary milestones

Program Plan

Phase I

Phase II



Phase I
Go/No-Go

BAA for
Phase II

Phase II
Go/No-Go

Microsystems Technology Office

Phase I Selected Program

Development of 3-inch and 4-inch Silicon Carbide Substrates, Epitaxy, and MW Class Power Devices	Cree, Inc.
Development of Megawatt SiC Power Switches for High Frequency Power Conversion Applications	Rockwell Scientific, LLC
Innovative SiC Materials Technologies for High Power Device Applications	Sterling Semiconductor
Development of Process Technologies for High-Performance MOS-Based SiC Power Switching Devices	Purdue University
Low Surface Field DMOS Structures for Discrete and Integrated High-Voltage Silicon Carbide Power MOS-Gated Bipolar Transistors with Trench Epitaxial Regrowth	Rensselaer Polytechnic Institute
Very Low Defect Density 4H-SiC Thin Films and their Application in High-Power Devices (a-plane growth at NCSU only)	North Carolina State University
Development of Critical 4H-SiC Processes for Demonstrating A Novel SiC Power Switch Capable of 10kV-100A	Rutgers University
Ferroelectrics on SiC for power switches	Georgia Tech
Government evaluation team	ARL, NRL, NIST

18 month base programs with 6 month option = 24 months

Summary

- WBG HPE will enable superior power systems for the future electric force.
- Material quality remains the critical challenge.
- Program success requires successful demonstration of critical milestones.
- Expanded device and circuit activities in Phase II will only occur if Phase I milestones are demonstrated.